AMENDMENTS TO THE CLAIMS

Please cancel claims 6, 13 and 15 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

a circuit configured to (i) monitor a plurality of signals for transitions and (ii) invert said signals only when at least a predetermined number of said signals transition to a particular logic state; and

a plurality of buffers configured to present said signals on a transmission bus, wherein said circuit comprises (i) a transition checker circuit directly receiving said signals and configured to present a plurality of transition signals each indicating a transition direction of one of said signals, (ii) a control circuit configured to present a flag signal when at least said predetermined number of said transition signals indicate said transition direction is to said particular logic state and (iii) an inverter circuit configured to invert said signals in response to said flag signal, wherein said transition checker circuit comprises (i) a plurality of flip-flops directly receiving said signals and configured to present said signals as a plurality of sampled signals, (ii) a plurality of inverters configured to present said signals as a plurality of inverted signals, and (iii) a plurality of logic gates configured to present said transition signals in response to said sampled signals and said inverted signals.

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said particular logic state is one of (i) a high logic state and (ii) a low logic state.

3. (ORIGINAL) The apparatus according to claim 1, wherein said predetermined number is greater than one half of a total number of said signals.

4. (CANCELED)

5. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said buffers are further configured to present said flag signal on said transmission bus.

6. (CANCELED)

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said circuit further comprises a plurality of first flip-flops configured to store said signals as presented by said inverter circuit.

8. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein said circuit further comprises a clock configured to present a clock signal to said first flip-flops.

9. (PREVIOUSLY PRESENTED) The apparatus according to claim 8, wherein said buffers are further configured to present said flag signal on said transmission bus and said transition checker circuit comprises:

a plurality of second flip-flops configured to present said signals as a plurality of sampled signals;

a plurality of inverters configured to present said signals as a plurality of inverted signals; and

a plurality of logical gates configured to present said transition signals in response to said sampled signals and said inverted signals.

10. (CURRENTLY AMENDED) A method of reducing noise induced by transitions of a plurality of signals, the method comprising the steps of:

(A) monitoring said signals for said transitions using a plurality of transition signals on a plurality of independent lines, each of said transition signals indicating a transition direction of one of said signals;

(B) inverting said signals only in response to at least a predetermined number of said signals transitioning to a particular logic state; and

(C) presenting said signals on a transmission bus, wherein step (A) comprises the sub-steps of (i) generating a plurality of transition signals each indicating a transition direction of one of said signals and (ii) generating a flag signal when at least said predetermined number of said transition signals indicate said transition direction is to said particular logic state, wherein generating said plurality of transition signals comprises the sub-steps of (a) sampling said signals to present a plurality of sampled signals, (b) inverting said signals to present a plurality of inverted signals and (c) logically combining said sampled signals and said inverted signals to present said transition signals.

11. (PREVIOUSLY PRESENTED) The method according to claim 10, wherein said particular logic state is one of (i) a high logic state and (ii) a low logic state.

12. (ORIGINAL) The method according to claim 10, wherein said predetermined number is greater than one half of a total number of said signals.

13. (CANCELED)

14. (CURRENTLY AMENDED) The method according to claim ~~13~~10, further comprising the step of presenting said flag signal on said transmission bus.

15. (CANCELED)

16. (CURRENTLY AMENDED) The method according to claim ~~15~~10, further comprising the step of storing said signals prior to presenting said signal on said transmission bus.

17. (ORIGINAL) The method according to claim 16, further comprising the step of generating a clock signal to control said storing.

18. (CURRENTLY AMENDED) An integrated circuit comprising:

means for monitoring a plurality of signals for transitions comprising means for presenting a plurality of transition signals on a plurality of independent lines, each of said transition signals indicating a transition direction of one of said signals;

means for inverting said signals only in response to at least a predetermined number of said signals transitioning ~~in a predetermined direction~~ to a particular logic state; and

means for presenting said signals on a transmission bus, wherein said means for monitoring comprises (i) generating a plurality of transition signals each indicating a transition direction of one of said signals and (ii) generating a flag signal when at least said predetermined number of said transition signals indicate said transition direction is to said particular logic state, wherein generating said plurality of transition signals comprises the sub-steps of (a) sampling said signals to present a plurality of sampled signals, (b) inverting said signals to present a plurality of inverted signals and (c) logically combining said sampled signals and said inverted signals to present said transition signals.

19. (PREVIOUSLY PRESENTED) The integrated circuit according to claim 18, wherein said predetermined direction is one of (i) a high to low direction and (ii) a low to high direction.

20. (CANCELED)